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To:	Examiner Aditya S. Bhat	From:	Timothy N. Trop
Company:	US Patent Office	Date:	January 17, 2006
Fax:	(571) 273-8300	Pages:	8 (including cover sheet)
Your Re:	10/660,310	Our Re:	ITL 1029US

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE JAN 17 2006

In re Applicant:	§	
Richard L. Coulson et al.	§	Art Unit: 2863
	§	
Scrial No.: 10/660,310	§	Examiner: Aditya S. Bhat
	§	
Filed: September 11, 2003	§	Docket: ITL.1029US
	§	P16765
For: Adaptive Cache Algorithm for	§	
Temperature Sensitive Memory	§	Assignee: Intel Corporation
	§	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL REPLY TO FINAL REJECTION

Sir:

In further response to the final rejection mailed October 25, 2005, please amend the above-referenced patent application as follows:

Date of Deposit: January 17, 2006
I hereby certify that this document is being facsimile transmitted to the United States Patent and Trademark Office (Fax No. 571/273-8700) on the date indicated above.
Cynthia L. Hayden
Cynthia L. Hayden